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COMPLEMENTARY METAL OXIDE SEMICONDUCTOR IMAGE SENSOR USING FIELD EFFECT TRANSISTOR TYPE PHOTODETECTOR FOR HIGH-SPEED BINARY OPERATION

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Abstract: In this paper, we propose a CMOS image sensor that uses a gate/body-tied p-chnnel metal oxide semiconductor field effect transistor (PMOSFET)-type photodetector for high- speed binary operation. The sensitivity of the gate/body-tied PMOSFET-type photodetector is approximately six times that of the p–n junction photodetector for the same area. Thus, an active pixel sensor with a highly sensitive gate/body-tied PMOSFET-type photodetector is more appropriate for high-speed binary operation. Moreover, the CMOS image sensor for binary operation has the advantages of low power consumption and a simple circuit because an analog- to-digital converter is not necessary. The proposed image sensor was fabricated and measured using a CMOS 0.35 μm conventional process.

Keywords: CMOS, image sensor, binary operation, gate/body-tied PMOSFET, photodetector

1. Introduction

The CMOS image sensor (CIS) has many advantages, such as low supply voltage, low hardware cost, and on-chip functionality.[1,2] Despite these advantages, difficulties arise inpixel design owing to the scaling down of the CMOS process.[3] In the conventional CIS, the active-pixel sensor (APS) is based on a p–n junction photodetector. However, many types of photodetectors have been developed for image sensors, including the bipolar junction transistor (BJT), hole accumulation diodes (HADs), silicon-on-insulator (SOI), and avalanche photodiode (APD).[4–6] Compared with these photodetectors, the gate/body-tied (GBT) p-channel metal oxide semiconductor field effect transistor (PMOSFET)-type photodetector implemented in this study is suitable for the CIS in the case of high-speed binary operation because it ishighly sensitive, occupies a small area of the APS, and features effective on-chip integration.[7] A single photon avalanche diode (SPAD)-based single photon counting image sensor was previously proposed for binary images.[8] However, the image sensor proposed in this paper is more effective for high image resolution since it has a smaller pixel size than the SPAD, which is based on a deep n-well layer. Moreover, high voltage, which is required for SPAD, is not required in the proposed image sensor.

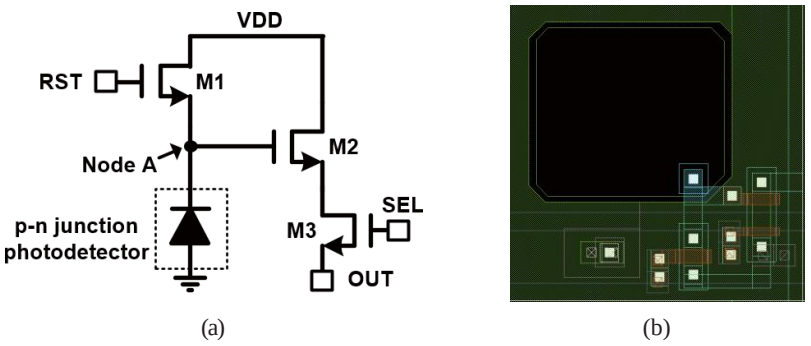
The multibit analog-to-digital converter (ADC) for a gray-scale image is integrated to digitize the analog signals of the APS in the conventional CIS. On the other hand, binary image sensors using a highly sensitive photodetector have been studied in recent years, and a gray-scale image can now be obtained using a binary image sensor via oversampling.[9,10]

In this paper, a CIS that uses a gate/body-tied PMOSFET-type photodetector for high-speed binary operation is proposed. The proposed CIS was fabricated using a 0.35 μm conventional

CMOS process, and its performance was measured and evaluated. By using the proposed CIS, a motion can be detected under the low illumination condition owing to the high-sensitivity PMOSFET-type photodetector. Edge detection can also be implemented by the binary operation. The proposed CIS has various applicatons such as barcoding and texture recognition, since they require only the white and black information.

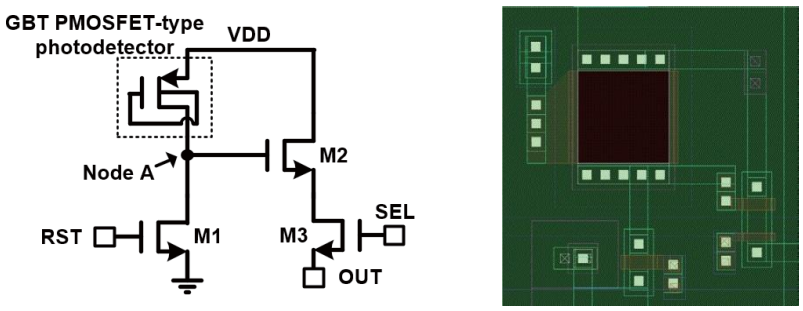
2. Design and Operating Principle

The designs of the APSs with the p–n junction photodetector and the GBT PMOSFET-type photodetector are shown in Figs. 1 and 2, respectively. These two APSs are based



(a) (b)

Fig. 1. (Color online) (a) Schematic diagram and (b) layout of the APS with the p–n junction photodetector.



(a) (b)

Fig. 2. (Color online) (a) Schematic diagram and (b) layout of the APS with GBT PMOSFET-type photodetector.

on three transistors (3-Tr) with dimensions of 13 × 13 μm^2. They are used to compare the characteristics of the measurement. The intensity of light incident on the photodetector without a shielding metal is converted into an electrical charge (Q_{ph}) in the 3-Tr APS. Subsequently, Q_{ph} is amplified by the GBT PMOSFET-type photodetector consisting of a PMOSFET and a gate (polysilicon) tied to the body (n-well). The n-well is commonly used as the body region of the PMOSFET and also used for photodetection in the GBT PMOSFET-type photodetector. The amplification factor (G_{GBT}) is defined as the ratio of Q_{ph} to the amplified electrical charge. The relationship between the output signal (V_{out}) of the APS and Q_{ph} in the p–n junction photodetector is given by Eq. (1), where G_{SF} is the source follower gain and C_A is the capacitance of the node A in the 3-Tr APS, and the relationship in the GBT PMOSFET-type photodetector is given by Eq. (2). Equations (1) and (2) are for rough estimation and conceptual representation.

$$V_{out} = \int_0^t I_{ph} dt \; G_{SF}/C_A = Q_{ph} G_{SF}/C_A \quad (1)$$

$$V_{out} = Q_{ph}G_{GBT}G_{SF}/C_A \quad (2)$$

The frame rate of the CIS is inversely proportional to the exposure time of the APS. The exposure time decreases as the frame rate increases. The APS with a highly sensitive GBT PMOSFET-type photodetector is suitable for binary image sensors with high frame rates, because the output signal of the APS is amplified in a short exposure time. The operational principle of the GBT PMOSFET-type photodetector is as follow. The charges generated by the incident light affect the potential at the gate and body, and these charges are amplified by the GBT PMOSFET-type photodetector.[11] As shown in Fig. 2, M1 resets the node A, M2 serves as a source follower for the readout of the pixel signal, and the pixel is selected by M3 at the end of each exposure time.

Figure 3 shows a block diagram of the CIS for binary operation. In the conventional CIS, the ADC is required to obtain multibit data, but the proposed CIS uses binary operation for 1-bit

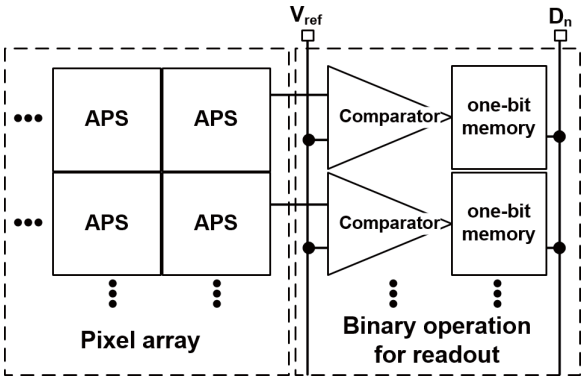


Fig. 3. Block diagram of the CIS for binary operation.

data (D_n) at a high frame rate. The block diagram is composed of two parts—a pixel array and a binary operation for the readout. The output signal of the APS in the pixel array is connected to the input of the comparator in the binary operation. In the comparator, the output signal of the APS is compared with a reference signal (V_{ref}), which is controllable. Furthermore, V_{ref} is the threshold for determining D_n in the binary operation, which is defined as Eq. (3).

$$D_n = \begin{cases} 1, & \text{if } V_{out} > V_{ref} \\ 0, & \text{otherwise} \end{cases} \quad (3)$$

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The output signals of the comparators are stored in the 1-bit memories and read out by the horizontal scanner. A white or black pixel in the output image is represented by the 1-bit data. The principle of the binary operation is shown in Fig. 4.

3. Measurement Results and Discussion

A photograph of the fabricated chip is shown in Fig. 5. The chip was manufactured using a CMOS 0.35 μm conventional process. It is composed of two pixel arrays, scanners, column parallel readouts, and biases. One pixel array is based on a GBT PMOSFET-type photodetector and the other pixel array is based on a p–n junction photodetector. The column-parallel readouts include the analogue readout circuits for the gray-scale image and the binary readout circuits for the binary image. The output data of the pixel array is read out by the column-parallel readouts, including the analogue and binary readout circuits. The size of the chip is 4 × 2.5 mm^2 and the resolution of the pixel arrays is 100 (V) × 144 (H).

The measurement results showing the variation in digital output as a function of light intensity are shown in Fig. 6. The measurement results of the GBT PMOSFET-type photodetector and the p–n junction photodetector were compared according to frame rate. The GBT PMOSFET-type photodetector is approximately six times more sensitive than the p–n junction photodetector and has a higher output voltage swing under 4000 lux at 120 fps (frames per second).

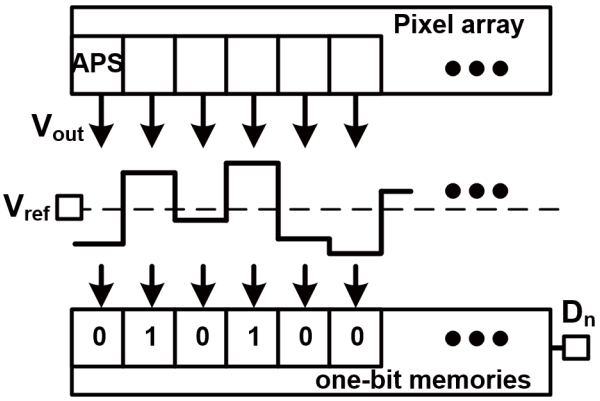


Fig. 4. Principle of the binary operation.

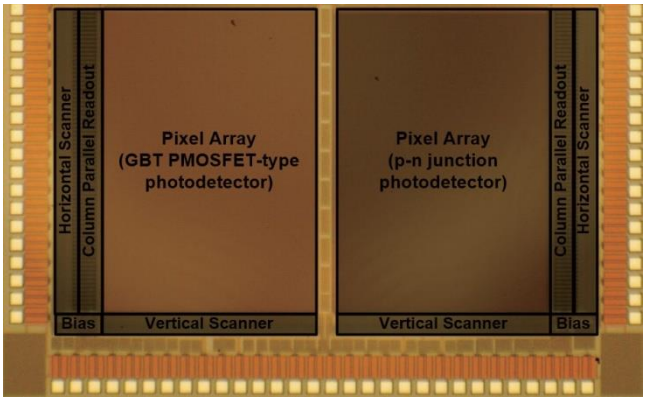


Fig. 5. (Color online) Photograph of the fabricated chip.

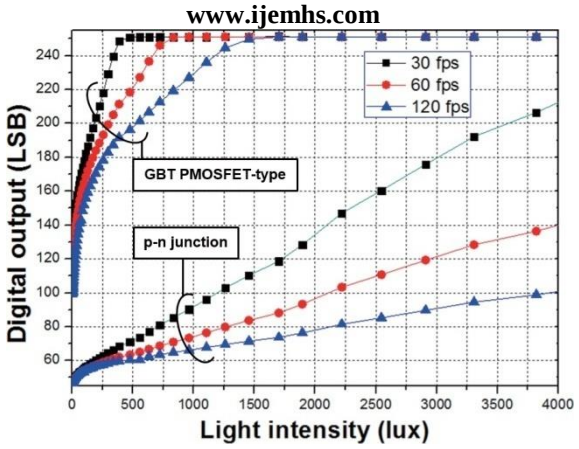
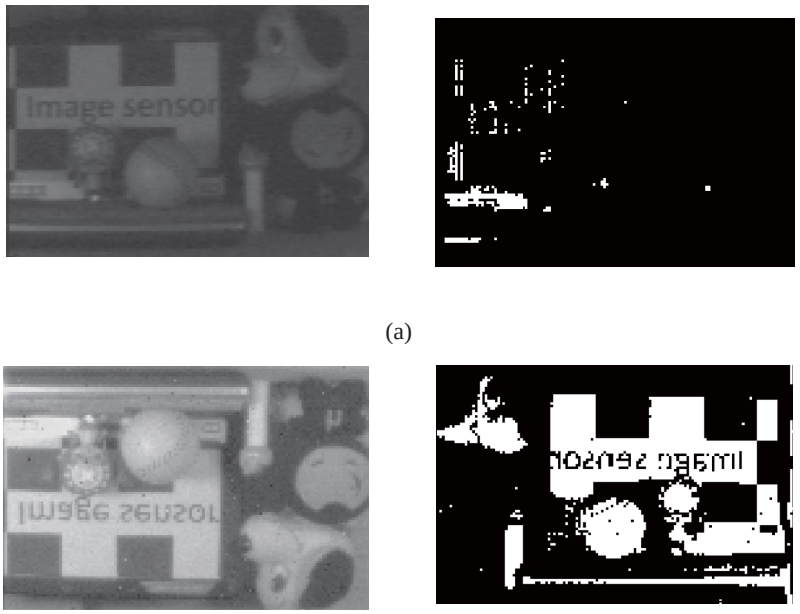


Fig. 6. (Color online) Measurement results showing the variation in digital output as a function of light intensity.



(a)

(b)

Fig. 7. Gray-scale and binary images produced by the image sensor at 120 fps: (a) p–n junction photodetector and (b) GBT PMOSFET-type photodetector.

Figure 7 shows the gray-scale and binary images produced by the image sensor at 120 fps under the same conditions. The gray-scale images have 8-bit output data, whereas the binary images have 1-bit output data and are represented by black and white pixels. The performance characteristics of the APSs with the p–n junction photodetector and GBT PMOSFET-type photodetector were compared. The primary focus is to measure the sensitivity and binary operation. The GBT PMOSFET-type photodetector exhibited better performance for binary operation (a 1-bit decision operation) than the p–n junction photodefector, because it is more sensitive, as shown in the gray-scale image. The overall characteristics of the proposed CIS are summarized in Table 1.

Table 1
Characteristics of the proposed CIS.

Process	CMOS 0.35 μm conventional process
Pixel size	13 × 13 μm^2

Pixel type	3-Tr APS with GBT PMOSFET-type and p–n junction photodetector
Number of pixels	100 (V) × 144 (H).
Power supply	3.3 V (digital and analog)
Size of chip	4×2.5 mm^2
Sensitivity	59.2 mV/lux·s (GBT PMOSFET-type) and 10.3 mV/lux·s (p–n junction)
Maximum frame rate	More than 2000 fps (binary) and 240 fps (gray scale)

4. Conclusions

An APS with a GBT PMOSFET-type photodetector was proposed in this paper for high-speed binary operation. The proposed APS has been designed and fabricated using a CMOS 0.35 μm conventional process. The proposed image sensor has a higher sensitivity and a simpler circuit than the conventional CIS with the multibit ADC for gray-scale images, and the GBT PMOSFET-type photodetector does not require the use of a special fabrication process for high sensitivity. The sensitivity of the APS with the GBT PMOSFET-type photodetector is higher than that with a p–n junction photodetector of the same size. We confirmed that the high-sensitivity GBT PMOSFET-type APS is better for high-speed binary operation than the conventional APS using a p–n junction photodetector.

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